IN THE CLAIMS:

Amendments to the Claims:

Please amend the claims as shown.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A display device having thin film transistors on a substrate thereof, wherein

the display device includes gate patterns, in each of which a gate line and a gate electrode of ~~the~~ a thin film transistor are integrally formed, and drain lines;

the gate pattern is constituted by at least three-layered films consisting of a lowermost layer, an intermediate layer formed of at least one layer and an uppermost layer at least at either a portion of the thin film transistor or a portion of the gate pattern which crosses a drain line~~,~~;

the intermediate layer is formed of a material selected from the group consisting of pure Al, an Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy, and the uppermost layer and the lowermost layer are formed of a metal having a melting point higher than ~~a~~ the melting point of the material of the intermediate layer~~,~~; and

end portions of the intermediate layer are ~~retracted~~ recessed from end portions of the uppermost layer and end portions of the lowermost layer.

2. (original) A display device according to claim 1, wherein the uppermost layer and the lowermost layer are formed of pure Mo or an Mo alloy.

3. (original) A display device according to claim 1, wherein the uppermost layer and the lowermost layer are formed of an Mo-W alloy.

4. (currently amended) A display device according to claim 1, wherein end portions of the uppermost layer ~~are retracted~~ spaced inwardly from end portions of the lowermost layer.

5. (original) A display device according to claim 1, wherein the thin film transistor includes a semiconductor layer and the gate electrode is arranged above the semiconductor layer.

6. (original) A display device according to claim 1, wherein the thin film transistor includes a polycrystalline semiconductor layer.

7. (currently amended) A display device having thin film transistors on a substrate thereof, wherein

the display device includes gate patterns, in each of which a gate line and a gate electrode of ~~the~~ a thin film transistor are integrally formed, drain lines, and an insulation film which covers the gate patterns~~,~~;

the gate pattern is constituted by at least three-layered films consisting of a

lowermost layer, an intermediate layer formed of at least one layer and an uppermost layer at least at either one of a portion of the thin film transistor or a portion of the gate pattern which crosses a drain line~~,~~;

the intermediate layer is formed of a material selected from the group consisting of pure Al, an Al alloy, pure Ag, an Ag alloy, pure Cu and a Cu alloy, and the uppermost layer and the lowermost layer are formed of a metal having a melting point higher than ~~a~~ the melting point of the material of the intermediate layer, and

end portions of the uppermost layer of the gate electrode are ~~retracted~~ spaced inwardly from end portions of the lowermost layer and, at the same time, end portions of the intermediate layer of the gate electrode are ~~retracted~~ recessed from end portions of the uppermost layer and end portions of the lowermost layer.

8. (original) A display device according to claim 7, wherein the thin film transistor includes a semiconductor layer and the gate electrode is arranged above the semiconductor layer.

9. (original) A display device according to claim 8, wherein the uppermost layer and the lowermost layer are formed of pure No or an Mo alloy.

10. (original) A display device according to claim 8, wherein the uppermost layer and the lowermost layer are formed of an Mo-W alloy.

11. (currently amended) A display device according to claim 8, wherein the

uppermost layer and the lowermost layer are formed of an Mo alloy, and ~~an~~ the etching rate of the Mo alloy of the uppermost layer is faster than ~~an~~ the etching rate of Mo alloy of the lowermost layer.

12. (original) A display device according to claim 11, wherein the lowermost layer is formed of an Mo-Cr alloy and the uppermost layer is formed of an Mo-W alloy.

13. (currently amended) A display device according to claim 7, wherein the semiconductor layer includes an LDD region, and the lowermost layer of the gate electrode has at least a portion thereof that is overlapped with the LCD region.

14. (original) A display device according to. claim 7, wherein the thin film transistor includes a polycrystalline semiconductor layer.